IN THE CLAIMS

Please amend the claims as follows:

1. (Original) An apparatus for modeling a power system of a microprocessor based system, comprising:

a plurality of power converter models;

a board model that receives an output from the plurality of power converter models;

a package model that receives an output from the board model; and

a chip model that receives an output from the package model.

2. (Original) The apparatus of claim 1, wherein the plurality of power converter models comprises a plurality of DC to DC power converter models.

3. (Original) The apparatus of claim 1, wherein the plurality of power converter models comprises four DC to DC power converter models.

4. (Original) The apparatus of claim 1, wherein the chip model further comprises:

a plurality of bump and grid models;

a plurality of section models that receives a plurality of outputs from the plurality of bump and grid models; and

a plurality of channel models that interconnect the plurality of section models.

5. (Original) The apparatus of claim 4, wherein the plurality of bump and grid models comprises nine bump and grid models.

6. (Original) The apparatus of claim 4, wherein each of the plurality of section models further comprises a load model.

7. (Original) The apparatus of claim 6, wherein the load model comprises a voltage controlled resistor.

8. (Original) The apparatus of claim 6, wherein the load model comprises a current source.

9. (Original) The apparatus of claim 4, wherein the plurality of section models are arranged in an interconnecting grid.

10. (Original) The apparatus of claim 9, wherein the interconnecting grid is generally square shaped.

11. (Original) The apparatus of claim 4, wherein the plurality of section models comprises nine section models.

12. (Currently Amended) The apparatus of claim 11, wherein the plurality of the section models are arranged in a three-section by three-section grid.

13. (Original) The apparatus of claim 4, wherein the plurality of the channel models comprises ten section models.

14. (Original) An apparatus for modeling a power system of a microprocessor based system, comprising:

means for modeling a power converter;

means for modeling a board that receives an output from the means for modeling a power converter;

means for modeling a package that receives an output from the means for modeling a board; and

means for modeling a chip that receives an output from the means for modeling a package.

15. (Original) A method for modeling a power system of a microprocessor based system, comprising:

modeling a plurality of power converters;

modeling a board that receives an output from the plurality of power converter;

modeling a package that receives an output from the board; and

modeling a chip that receives an output from the package.

16. (Original) The method of claim 15, wherein the plurality of power converters

comprises four DC to DC power converters.

17. (Original) The method of claim 15, wherein modeling a chip that receives an output from the package further comprises:

modeling a plurality of bump and grid components;

modeling a plurality of chip sections that receives an output from the plurality of bump and grid components; and

modeling a plurality chip channels that interconnects the plurality of chip sections.

18. (Original) The method of claim 17, wherein modeling a plurality of chip sections forms a generally square shaped grid.

19. (Currently Amended) The method of claim 18, wherein the generally square shaped grid comprises a three-section by three-section grid.

20. (Original) The method of claim 17, wherein modeling a plurality of chip sections further comprises modeling a load.

21. (Original) The method of claim 20, wherein the load is modeled as a voltage controlled resistor.

22. (Original) The method of claim 20, wherein the load is modeled as a current

source.

23. (Original) An apparatus for modeling a power system of a microprocessor chip, comprising:

a plurality of bump and grid models;

a plurality of section models that receives a plurality of outputs from the plurality of bump and grid models; and

a plurality of channel models that interconnect the plurality of section models.

24. (Original) The apparatus of claim 23, wherein the plurality of section models further comprises a load model.

25. (Original) The apparatus of claim 24, wherein the load model further comprises a voltage controlled resistor.

26. (Original) The apparatus of claim 24, wherein the load model further comprises a current source.

27. (Original) The apparatus of claim 23, wherein the plurality of section models are arranged in an interconnecting grid.

28. (Original) The apparatus of claim 27, wherein the interconnecting grid in

generally square shaped.

29. (Original) The apparatus of claim 23, wherein the plurality of section models comprises nine section models.

30. (Currently Amended) The apparatus of claim 29, wherein the plurality of section models are arranged in a three-section by three-section grid.

31. (Original) An apparatus for modeling a power system of a microprocessor chip, comprising:

means for modeling a plurality of bumps and grids;

means for modeling a plurality of sections that receives a plurality of outputs from the plurality of bumps and grids; and

means for modeling a plurality of channels that interconnect the plurality of sections.

32. (Original) A method for modeling a power system of a microprocessor chip, comprising:

modeling a plurality of bump and grid components;

modeling a plurality of chip sections that receives an output from the plurality of bump and grid components; and

modeling a plurality chip channels that interconnect the plurality of chip sections.

33. (Original) The method of claim 32, wherein modeling a plurality of chip sections forms a generally square shaped grid.

34. (Currently Amended) The method of claim 33, wherein the generally square shaped grid is a three-section by three-section grid.

35. (Original) The method of claim 32, wherein modeling a plurality of chip sections further comprises modeling a load.

36. (Original) The method of claim 35, wherein the load is modeled as a voltage controlled resistor.

37. (Original) The method of claim 35, wherein the load is modeled as a current source.